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KW11-P programmable real-time clock user's manual (Etch Rev F and up)

digital

EK-KW1PF-OP-001

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CHAPTER 1
INTRODUCTION

1.1 GENERAL

The KW11-P Programmable Real-Time Clock is an option for the PDP-11 system which provides a method of accurately measuring time intervals. The KW11-P consists of a quad-height module (M7228) that provides programmed real-time interval interrupts and interval counting in several modes of operation. Addition of this module to a PDP-11 system allows hardware interval counting, which reduces program instruction time and allows more efficient use of computer time.

Although signals are transferred between the KW11-P module and the Unibus, this manual does not describe the operation of the Unibus. A detailed description of the Unibus is presented in the *PDP-11 Peripherals Handbook*.

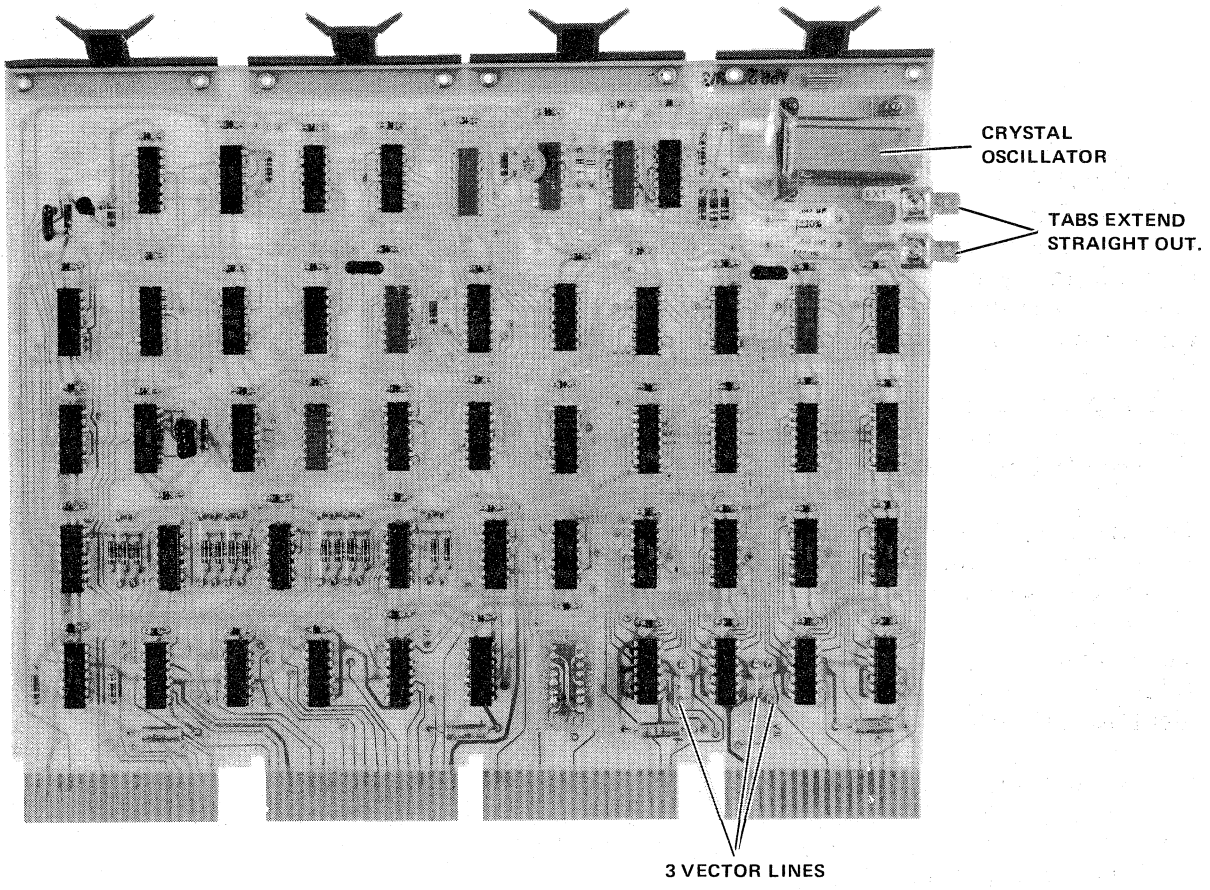
This manual provides the user with the theory of operation necessary to understand and maintain the KW11-P Programmable Real-Time Clock. The level of discussion assumes that the reader is familiar with basic digital computer theory.

The manual is organized into three chapters: Introduction, General Description, and Programming Information. A set of engineering logic drawings is provided with each KW11-P. The drawing set is identified as D-CS-M7228-0-1, Revision J, Sheets 1 through 5.

Sheet 1 – Component Placement and Parts Reference (KW-1)
Sheet 2 – Clock Control, Counter Control, and Control and Status Register (KW-2)
Sheet 3 – Counter and Count Set Buffer (KW-3)
Sheet 4 – Interrupt Control (KW-4)
Sheet 5 – Address Control (KW-5)

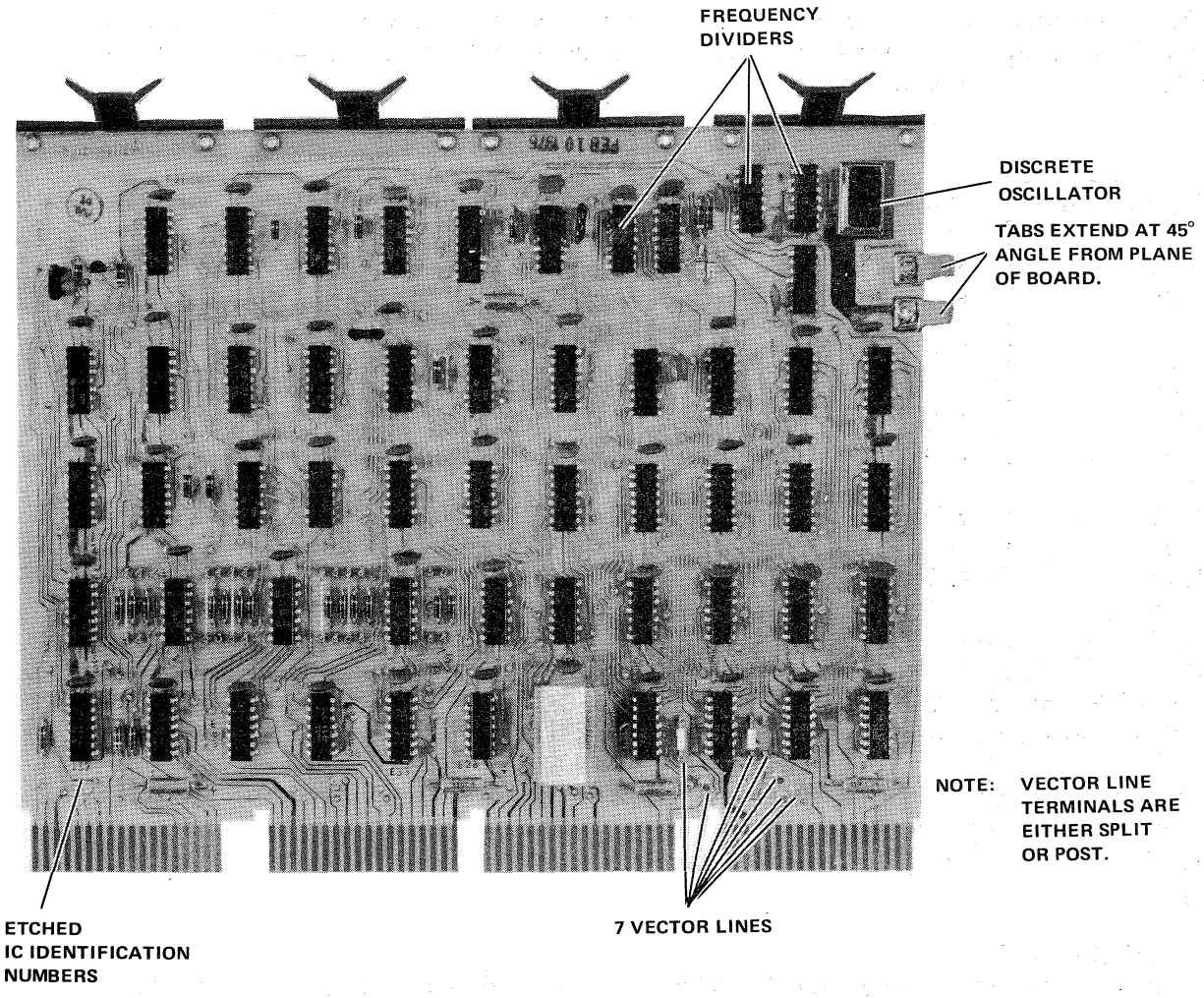
1.2 IDENTIFICATION OF MODULE

This manual provides a discussion of KW11-P boards of etch level F and higher, (see Figure 1-1) due to chip designation and circuit changes. Previously manufactured boards require corresponding documentation (EK-KW11P-MM-002).



Below Etch Level F

Figure 1-1 KW11-P Module Identification (Sheet 1 of 2)



Etch Level F and Above

Figure 1-1 KW11-P Module Identification (Sheet 2 of 2)

1.3 INSTALLATION

The KW11-P module plugs into an SPC slot. A wire must be installed to pick up the LTC L signal from the power supply and apply it to the line frequency input of the KW11-P.

When installed, the LTC L input to the KW11-P is located on pin CE1 and CD1. Connect a length of 30 AWG wire from one pin (CE1 or CD1 on the backplane) to the pin on the backplane, as designated in Table 1-1, for each application.

Table 1-1 LTC L Connection

PDP Computer	Processor	Pin Number
11/04	KD11-D (4 slot)	C02D1, C03D1, C04D1
11/04	KD11-D (9 slot)	C02D1, C03D1, C04D1, C05D1, C06D1, C07D1, C08D1, or C09D1
11/05	KA11-A w/8K memory	C01D1, C02D1, C03D1, C04D1, or F08V2
11/05	KD11-A w/16K memory	C01D1 or F08V2
11/20	KA11	A13P2 or B12R1
11/34	KD11-E	C03D1, C04D1, C05D1, C06D1, C07D1, C08D1, or C09D1
11/35	KD11-A	F03R1 or C09D1
11/40	KD11-A	F03R1 or C09D1
11/45	KB11-A	C26D1, C27D1, or C28D1
11/55	KB11-D	C26D1, C27D1, or C28D1
11/70	KB11-B	C40D1, C41D1, C42D1, C43D1, or C44D1
11/70	KB11-C	C40D1, C41D1, C42D1, C43D1, or C44D1
DD11-B Peripheral Mounting Panel		C01D1, C02D1, C03D1, or C04D1
DD11-D Peripheral Mounting Panel		C01D1, C02D1, C03D1, C04D1, C05D1, C06D1, C07D1, C08D1, C09D1

NOTE: A wire connection is not necessary for backplane pin numbers ending in D1. LTC L is already connected to the line frequency input of the KW11-P.

1.4 DIAGNOSTIC

A diagnostic paper tape program (MAINDEC-11-DZKWB-G-D) is provided with the KW11-P. This program tests the KW11-P Real-Time Clock. It contains a series of incremental routines that test the Control and Status Register, Count Set Buffer, Counter, and Interrupt Vector Address using 100 kHz, 10 kHz, and line frequencies. For a detailed description of the diagnostic, see the diagnostic listing (also provided).

CHAPTER 2
GENERAL DESCRIPTION

2.1 INTRODUCTION

The KW11-P provides programmed real-time interval interrupts and interval counting in several modes of operation. It is a quad-height module (M7228) that is installed in an SPC slot. A wide range of system programming requirements can be met with the KW11-P.

It operates in the single-interrupt mode, and the repeat-interrupt mode, and also functions as an external event counter. Four selectable clock rates include: 100 kHz, 10 kHz, line frequency, and external clock.

This chapter presents an overview of the KW11-P operation. The discussion is keyed to the block diagram level.

2.2 FUNCTIONAL UNITS

The major functional units of the KW11-P include an Address Control, Interrupt Control, 16-bit Count Set Buffer, 16-bit synchronous binary up/down Counter, 9-bit Control and Status Register, and Clock and Clock Control (Figure 2-1).

Address Control

The Address Control decodes address information from the Unibus and provides gating signals for the selected element (status register, buffer, or counter).

Interrupt Control

The Interrupt Control permits the KW11-P to gain control of the bus (become bus master) and perform an interrupt operation. Single interrupts or repeated interrupts are generated, depending on the mode selected (see Paragraph 2.3).

Count Set Buffer and Counter

The Count Set Buffer receives the preset interval count from the bus via Unibus receivers. Coincident with a load pulse, all 16 bits of input data are transferred to the buffer output. The Counter inputs are connected directly to the buffer outputs. The Counter is now loaded with a preset interval count and is ready for operation. The preset interval count is also retained in the buffer. The Counter will count up or down by clock pulses until overflow or underflow, which is detected by interrupt control. The Counter outputs are connected to the bus with Unibus drivers. A control signal to the drivers transfers the Counter output to the bus so it can be read during operation.

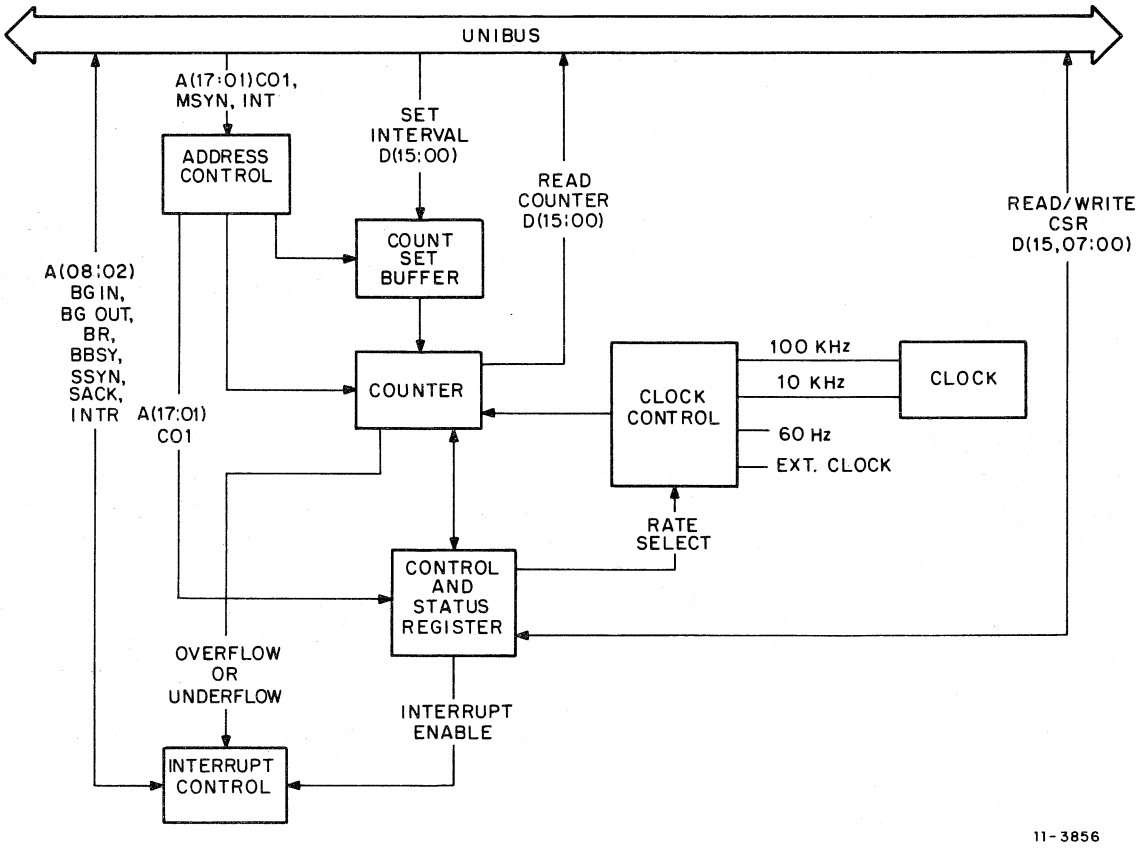


Figure 2-1 KW11-P Programmable Real-Time Clock, Simplified Block Diagram

Control and Status Register

The overall operation of the KW11-P is controlled by signals from the Control and Status Register. This 9-bit register responds to programmed information from the processor. It generates signals to provide the following functions.

1. Select Single or Repeat Interrupt (MODE).
2. Start Counter/Stop Counter (RUN).
3. Control count up/down (UP/DN).
4. Control count rate: 100 kHz, 10 kHz, 60 Hz, or external clock (RATE SELECT).
5. Indicate Counter overflow or underflow (DONE).
6. Provide an interrupt enable signal to interrupt control logic (INTR ENB).
7. Provide an error signal if a second underflow or overflow occurs in the repeat-interrupt mode before the interrupt generated by the previous underflow or overflow has been serviced (ERR).
8. Provide a signal to single-step the Counter for maintenance purposes (FIX).

Clock and Clock Control
Count pulses are generated from a crystal oscillator at a base frequency of 10 MHz. This base frequency is divided to generate the available 100 kHz and 10 kHz clock pulses. A signal is provided by the PDP-11 processor power supply as the line frequency (50/60 Hz) count rate. An external clock signal can also be used.

Both the external clock and line frequency signals are conditioned by Schmitt triggers. A clock selector/multiplexer provides the desired clock rate in accordance with programmed information from the Control and Status Register.

2.3 MODES OF OPERATION

The KW11-P has two program-selectable modes of operation:

Single-Interrupt Mode
A program-specified time interval preset and an interrupt is generated at the end of the interval. The time interval, represented as a specific count, is loaded into the Counter. Count down or count up is initiated at one of four selectable rates, and at underflow or overflow, an interrupt is generated. The clock is stopped and the Counter is reset to zero.

Repeat-Interrupt Mode
A program-specified time interval is preset and repeated interrupts are generated at a rate corresponding to the time interval. The time interval, represented as a specific count, is loaded into the Counter. Count down or count up is initiated, and at underflow or overflow, an interrupt is generated. The Counter is automatically reloaded from the Count Set Buffer and the clock is restarted. At the second underflow or overflow, another interrupt is generated. The sequence is repeated to produce a series of interrupts at program-specified intervals.

It is possible for a non-recoverable error to occur if the Counter underflows or overflows before the previous interrupt has been serviced.

2.4 SPECIFICATIONS

Electrical
+5.0 V (±0.25 V) @ 1.0 A, typically (power is supplied by the SPC slot).

Environmental
Temperature: 5° C – 50° C
Humidity: 10% – 95% non-condensation

External Frequency Input
TTL-compatible
100 kHz max (50% duty cycle)

Accuracy
0.01% overall, plus synchronization error and resolution of clock.

CHAPTER 3
PROGRAMMING INFORMATION

3.1 INTRODUCTION

This chapter provides programming rules and three sample programs for software control of the KW11-P. For detailed PDP-11 programming information, refer to the *Paper Tape Software Programming Handbook,* DEC-11-XPTSA-A-D.

3.2 PROGRAMMING RULES

The following programming rules must be followed:

1. Read the Counter prior to stopping it. Stopping the Counter might change its contents. If it is necessary to start the Counter from a previous value, save the value which was read, and reload it into the Count Set Buffer.

2. Do not loop on a Counter read command.

3. Note that the module is equipped with a hardware synchronization feature, which will add from 1/2 up to 1-1/2 clock intervals (of the selected rate) to the anticipated count time on the first interrupt, after the RUN bit is asserted.

3.3 PROGRAMMING EXAMPLES

The following three sample programs have been executed on a PDP-11 system. Example 1 demonstrates the KW11-P single interrupt mode of operation and Example 2 demonstrates the repeat interrupt mode of operation. Example 3 demonstrates the use of the KW11-P as an external interval timer. Example 4 demonstrates the use of the KW11-P as an external event counter.

KW11-P PROGRAMMING EXAMPLES

```
001000                  .=1000
172540          CSR=172540              ;CONTROL AND STATUS REGISTER
172542          CSB=172542              ;COUNT SET BUFFER
172544          CTR=172544              ;COUNTER
000240          NOP=240
001000          STACK=1000
002000          SAV=2000
```

EXAMPLE 1

```
                ;THIS DEMONSTRATES THE USE OF THE SINGLE INTERRUPT MODE TO CAUSE A
                ;PROGRAM INTERRUPT AFTER A SPECIFIED TIME INTERVAL. THE CLOCK FREQUENCY FOR
                ;THIS CASE COULD BE EITHER INTERNAL OR EXTERNAL.

001000 012767 001044 177076 EX1:    MOV     #EX1A,104       ;INITIALIZE INTERRUPT RETURN
001006 012767 000340 177072         MOV     #340,106        ;INITIALIZE NEW PROCESSOR STATUS AFTER INTERRUPT
001014 012706 001000                MOV     #STACK,%6       ;INITIALIZE STACK POINTER
001020 012767 000200 176750         MOV     #200,177776     ;SET PROCESSOR PRIORITY TO LEVEL 4
001026 012767 000074 171506         MOV     #60,,CSB        ;INITIALIZE COUNT SET BUFFER TO 60 (1 SECOND AT 60 HZ)
001034 012767 000105 171476         MOV     #105,CSR        ;SINGLE INTERRUPT ENABLED,COUNT DOWN, 60HZ, START CLOCK
001042 000001                       WAIT                    ;WAIT FOR INTERRUPT (OR OTHER USER CODE HERE)
                        ;USER CODE RESUMES HERE

001044 000240               EX1A:   NOP                     ;USER CODE TO HANDLE INTERRUPT BEGINS HERE
001046 000002                       RTI                     ;RETURN TO PROGRAM
```

EXAMPLE 2

```
                ;THIS DEMONSTRATES THE USE OF THE REPEAT INTERRUPT MODE TO CAUSE A
                ;PROGRAM INTERRUPT AFTER A SPECIFIED TIME INTERVAL REPEATEDLY. THE CLOCK FREQUENCY FOR
                ;THIS CASE COULD BE EITHER INTERNAL OR EXTERNAL.

001000 012767 001044 177076 EX2:    MOV     #EX1A,104       ;INITIALIZE INTERRUPT RETURN
001006 012767 000340 177072         MOV     #340,106        ;INITIALIZE NEW PROCESSOR STATUS AFTER INTERRUPT
001014 012706 001000                MOV     #STACK,%6       ;INITIALIZE STACK POINTER
001020 012767 000200 176750         MOV     #200,177776     ;SET PROCESSOR PRIORITY TO LEVEL 4
001026 012767 000074 171506         MOV     #60,,CSB        ;INITIALIZE COUNT SET BUFFER TO 60 (1 SECOND AT 60HZ)
001034 012767 000115 171476         MOV     #115,CSR        ;REPEAT INTERRUPT ENABLED,COUNT DOWN, 60 HZ, START CLOCK
001042 000001                       WAIT                    ;WAIT FOR INTERRUPT (OR OTHER USER CODE HERE)
                        ;USER CODE RESUMES HERE

001044 000240               EX1A:   NOP                     ;USER CODE TO HANDLE INTERRUPT BEGINS HERE
001046 000002                       RTI                     ;RETURN TO PROGRAM
```

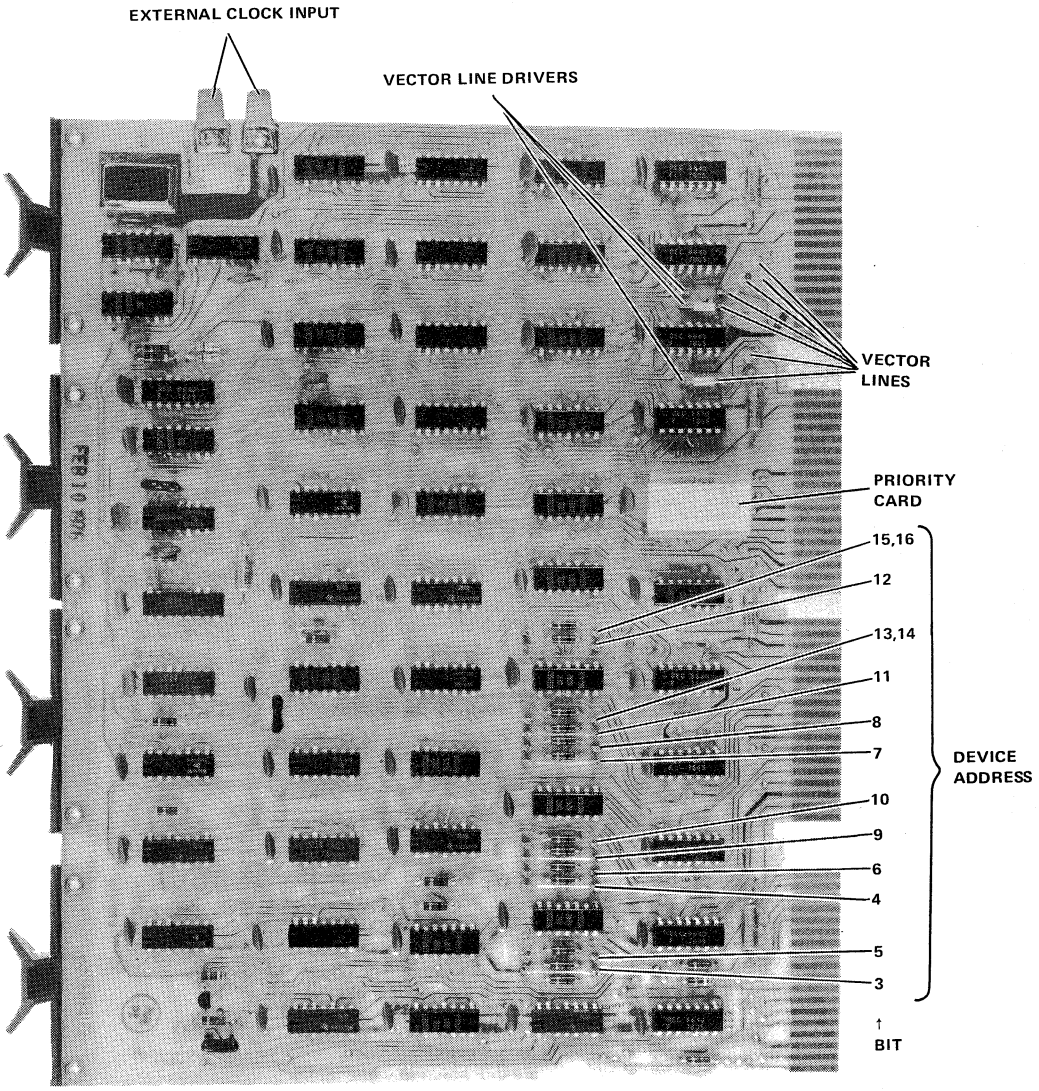
EXAMPLE 3

```
                        ;THIS DEMONSTRATES THE USE OF THE CLOCK AS AN EXTERNAL INTERVAL TIMER.
                        ;THE INTERRUPT IS NOT ENABLED. THE COUNTER IS READ TO DETERMINE TOTAL ELAPSED TIME.

001050 005067 171466    EX3:    CLR     CSB             ;CLEAR COUNT SET BUFFER
001054 012737 000021 172540     MOV     #21,@#CSR       ;COUNT UP, 100KHZ, START CLOCK
                        ;USER CODE HERE TO DETERMINE START AND FINISH OF EVENT.
001062 013737 172544 002000     MOV     @#CTR,@#SAV     ;STORE COUNTER CONTENTS.
001070 042737 000001 172540     BIC     #1,@#CSR        ;EVENT FINISHED, STOP CLOCK
                        ;ELAPSED TIME IS EQUAL TO VALUE IN SAV MULTIPLIED BY 10 MICROSECONDS.
                        ;CARE SHOULD BE TAKEN TO INSURE THAT THE ELAPSED TIME IS NOT SO LONG
                        ;AS TO CAUSE THE COUNTER TO OVERFLOW.
```

EXAMPLE 4

```
                        ;THIS DEMONSTRATES THE USE OF THE CLOCK AS AN EXTERNAL EVENT COUNTER.
                        ;THE INTERRUPT IS NOT ENABLED. THE COUNTER IS READ TO DETERMINE TOTAL NUMBER OF EVENTS.

001070 005067 171446    EX4:    CLR     CSB             ;CLEAR COUNT SET BUFFER
001074 012737 000027 172540     MOV     #27,@#CSR       ;COUNT UP, EXTERNAL FREQUENCY, START CLOCK.
                        ;USER CODE HERE TO DETERMINE INTERVAL SURROUNDING EVENTS TO BE COUNTED.
001102 013737 172544 002000     MOV     @#CTR,@#SAV     ;STORE COUNTER CONTENTS.
001110 042737 000001 172540     BIC     #1,@#CSR        ;STOP CLOCK.
                        ;TOTAL NUMBER OF EVENTS IS INDICATED BY VALUE IN SAV (SAV=002000)
        000001                  .END
```

APPENDIX A
KW11-P MODULE



	DEVICE ADDRESS	VECTOR LINES
JUMPER IN =	0	1
JUMPER OUT =	1	0

7915-1

KW11-P Module (M7228)

Reader's Comments

KW11-P PROGRAMMABLE REAL-TIME CLOCK
USER'S MANUAL (Etch Rev F and up)
EK-KW1PF-OP-001

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